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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,186	09/12/2000	Dong Yeung Kwak	8733.298.00	6720

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EXAMINER

LOKE, STEVEN HO YIN

ART UNIT PAPER NUMBER

2811

DATE MAILED: 08/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/660,186

Applicant(s)

KWAK, DONG YEUNG

Examiner

Steven Loke

Art Unit

2811

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 May 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-7 and 9-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2-7 and 9-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 16 May 2002 is: a) ☐ approved b) ☒ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5. 6) ☐ Other:

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 5/16/02 have been disapproved because they introduce new matter into the drawings. 37 CFR 1.121(a)(6) states that no amendment may introduce new matter into the disclosure of an application. The original disclosure does not support the showing of Δ in fig. 2A. The proposed drawing corrections of figs. 2B and 3 are approved.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 2 and 4-7 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Ono et al.

In regards to claim 2, Ono et al. shows all the elements of the claimed invention in figs. 1-3. It is a TFT LCD (thin film transistor liquid crystal display) comprising: a first substrate [SUB1] and a second substrate [SUB2]; a scanning

line [GL] on the first substrate; a signal line [DL] formed to cross the scanning line, wherein the signal line does not include an extension pattern; a channel layer [AS] formed along the signal line [DL] and extended to a portion of the scanning line [GL]; source and drain electrodes [SD1, DL] formed separated on the channel layer [AS] over the scanning line [GL]; a pixel electrode [ITO1] ← connected to the source electrode [SD1]; and a liquid crystal layer [LC] formed between the first substrate [SUB1] and the second substrate [SUB2]; wherein the drain electrode [DL] is parallel to the signal line [DL].

It is inherent that a pixel electrode connected to the drain electrode because the source and drain electrodes in the liquid crystal display device alternate with each other when the polarities are reversed during operation (col. 4, lines 56-64). Therefore, [SD1] becomes the drain electrode and [DL] becomes the source electrode when the polarities are reversed during operation.

In regards to claim 4, Ono et al. further discloses a gate insulating layer [GI] between the scanning line [GL] and the channel layer [AS].

In regards to claim 5, Ono et al. further discloses an ohmic contact layer [d0] between the source and drain electrodes [DL, SD1] and the channel layer [AS] when the polarities are reversed during operation.

In regards to claim 6, Ono et al. further discloses the source electrode [DL] and the signal line [DL] are formed as a unit when the polarities are reversed during operation.

Art Unit: 2811

In regards to claim 7, Ono et al. further discloses the drain electrode [SD1] is overlapped with the scanning line [GL] when the polarities are reversed during operation.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3 and 9-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al.

In regards to claims 3, 11, 17, Ono et al. further discloses the channel layer [AS] has a width smaller than a width of the scanning line [GL].

It would have been obvious for the channel layer has a width smaller than a width of the signal line because it depends to the desired resistance of the channel layer.

In regards to claim 9, Ono et al. discloses a TFT in figs. 1-3. It is a TFT LCD comprising: a first substrate [SUB1] and a second substrate [SUB2]; a plurality of scanning lines [GL] on the first substrate; a gate insulating layer [GI] on a surface inclusive of the scanning lines [GL]; a channel layer [AS] on the gate insulating layer to cross the scanning lines [GL] having a portion extended to a top of each of the scanning lines [GL]; source and drain electrodes [SD1, DL] formed separated on the channel layer [AS] over the scanning lines [GL]; the signal line [DL] does not include an extension pattern; a protection film [PSV1]

formed on a surface inclusive of the signal line [DL]; a pixel electrode [ITO1] connected to the source electrode [SD1] on the protection film; a liquid crystal layer [LC] formed between the first substrate [SUB1] and the second substrate [SUB2]; wherein the drain electrode [DL] is parallel to the signal line [DL].

It is inherent that a pixel electrode connected to the drain electrode because the source and drain electrodes in the liquid crystal display device alternate with each other when the polarities are reversed during operation (col. 4, lines 56-64). Therefore, [SD1] becomes the drain electrode and [DL] becomes the source electrode when the polarities are reversed during operation. The signal line [DL] formed as a unit with the source electrode [DL] along the channel layer [AS], which is formed to cross each of the scanning lines [GL] when the polarities are reversed during operation.

It would have been obvious for the gate insulating layer on an entire surface inclusive of the scanning lines because it protects the TFTs.

It would have been obvious for the protection film formed on an entire surface inclusive of the signal line because it protects the TFTs .

In regards to claim 10, Ono et al. further discloses the drain electrode [SD1] crosses the scanning line [GL] when the polarities are reversed during operation.

In regards to claim 12, Ono et al. further discloses an ohmic contact layer [d0] between the source and drain electrodes [DL, SD1] and the channel layer when the polarities are reversed during operation.

In regards to claim 13, Ono et al. further discloses the scanning line [GL] has a portion enlarged in the vicinity of the signal line [DL].

In regards to claim 14, Ono et al. further discloses the channel layer [AS] is formed along the signal line [DL] over the scanning line [GL]. It would have been obvious for the channel layer has a width enlarged as much as a width of the scanning line is enlarged because it depends to the desired resistance of the channel layer.

In regards to claim 15, Ono et al. shows a TFT in figs. 1-3. It is a TFT LCD having a first substrate [SUB1], a second substrate [SUB2], and liquid crystal [LC] sealed between the first and second substrates, comprising: a scanning line [GL] on the first substrate; a gate insulating layer [GI] on the scanning line [GL]; a channel layer [AS] on the gate insulating layer; a signal line [DL] formed to cross the scanning line [GL] to cover a portion of the channel layer [AS], wherein the signal line [DL] does not include an extension pattern.

It is inherent that a pixel electrode connected to the drain electrode because the source and drain electrodes in the liquid crystal display device alternate with each other when the polarities are reversed during operation (col. 4, lines 56-64). Therefore, [SD1] becomes the drain electrode and [DL] becomes the source electrode when the polarities are reversed during operation. The drain electrode [SD1] formed on the channel layer [AS] spaced a distance away from the signal line [DL] in parallel to the signal line [DL]. The protection film [PSV1] formed on a surface of the first substrate inclusive of the drain electrode [SD1]; a pixel electrode [ITO1] formed on the protection film connected to the drain electrode [SD1]; and the drain electrode [SD1] is parallel to the signal line [DL].

It would have been obvious for the protection film formed on an entire surface of the first substrate inclusive of the drain electrode because it protects the TFT.

In regards to claim 16, Ono et al. further discloses the channel layer [AS] is formed along the signal line [DL].

In regards to claim 18, Ono et al. further discloses the signal line [DL] serves as a source electrode disposed opposite to the drain electrode when the polarities are reversed during operation.

In regards to claim 19, Ono et al. further discloses a gate insulating layer [GI] between the scanning line [GL] and the channel layer [AS].

In regards to claim 20, Ono et al. further discloses an ohmic contact layer [d0] between the source and drain electrodes [DL, SD1] and the channel layer when the polarities are reversed during operation.

6. Applicant's arguments with respect to claims 2-7 and 9-20 have been considered but are moot in view of the new ground(s) of rejection.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**.

See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory

action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

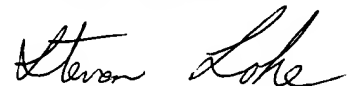
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
August 6, 2002

Steven Loke
Primary Examiner

A handwritten signature in cursive script that reads "Steven Loke".